a trench between said second bottom capacitor plate and said third bottom capacitor plate;

a common top capacitor plate over said first bottom capacitor plate, said second bottom capacitor plate, and said third bottom capacitor plate, wherein said top capacitor plate extends toward said contact at a first level within said array, the top capacitor plate includes a lateral clearance opening at the first level around the contact and does not vertically descend between each of the first, second and third bottom capacitor plates and the contact, and wherein said top capacitor plate lines a side of said trench and further lines a bottom of said trench at a second level within said array; and

a dielectric between said top capacitor plate and said first, second, and third bottom capacitor plates.

14. (Original) The array in claim 13, wherein said top capacitor plate extends toward a top of said contact.

Claims 15 - 66 (cancelled)

67. (Currently amended) An array of capacitors comprising:

first, second and third memory cell capacitors comprising first, second and third bottom container-shaped electrodes, respectively;

a bit line contact laterally positioned between the first and second memory cell, the bit line contact downwardly extends from a vertical height above a top of the first and second bottom electrodes;

a trench laterally positioned between the second and third bottom electrodes;

a common top electrode capacitively coupled to the first, second and third bottom electrodes via a capacitor dielectric layer, wherein the top electrode includes a lateral clearance opening above the top of the first bottom electrode and around the bit line contact, the top electrode is capacitively coupled to an interior of the first, second and third bottom electrodes

and a portion of the exterior of the second and third bottom electrodes located only in the trench; and

a bit line contact insulation region surrounding the bit line contact and filling a region between the bit line contact and the bottom electrode.

68. (Previously added, previously amended) An array of capacitors comprising:

first, second and third memory cell capacitors comprising first, second and third bottom container-shaped electrodes, respectively;

a bit line contact laterally positioned between the first and second memory cell, the bit line contact downwardly extends from a vertical height above a top of the first and second bottom electrodes;

a trench laterally positioned between the second and third bottom electrodes;

a common top electrode capacitively coupled to the first, second and third electrodes via a capacitor dielectric layer, wherein the top electrode includes a lateral clearance opening around the bit line contact, the top electrode is capacitively coupled to an interior of the first, second and third bottom electrodes and a portion of the exterior of the second and third bottom electrodes located in the trench; and

a bit line contact insulation region surrounding the bit line contact and filling a region between the bit line contact and the first and second bottom electrodes, wherein the bit line contact insulation region prevents the top electrode from downwardly extending between the bit line contact and the first and second bottom electrodes.